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(54) Clock generators for magnetic disk drives.

(57) A magnetic disk drive of the zone-bit recording type, in which a training signal is written in a preamble portion of data, has a clock generator comprising : a sample-holder circuit (61) for generating a sampling signal (Yn) from a read signal ; a phase-comparator (90) for detecting a phase difference (Zn) from the sampling signal ; a loop filter (68) ; and a voltage-controlled oscillator (69) whose frequency is controlled by the phase difference (Zn) as it is smoothed. The clock generator also comprises a frequency divider (11) ; a clock extraction circuit (12) for extracting a clock timing from the training signal as it is partially equalised ; and a phase-comparator (13) for finding a phase difference between an output of the frequency divider (11) and an output of the clock extraction circuit (12). The phase-comparator (13) is connected to the loop filter (68) during reproduction of the preamble portion of the data, and the partial-response phase-comparator (90) is connected to the loop filter (68) during reproduction of a data portion of the data, by the switching of a change-over switch (14). As a result, hangup is prevented and an accurate clock timing is promoted in the clock generator.

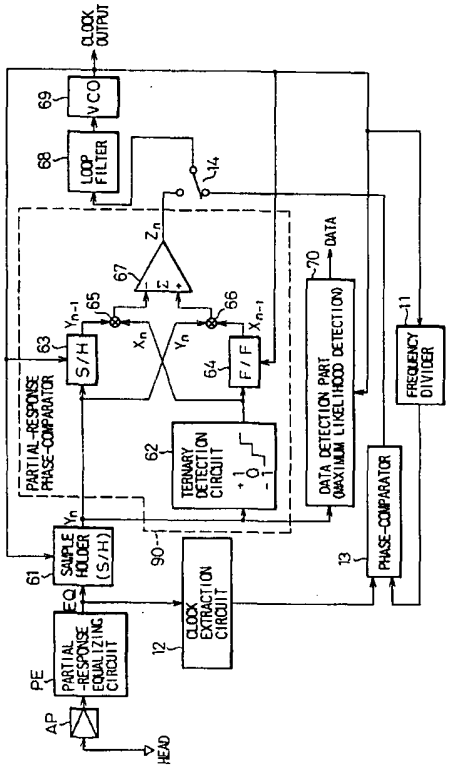

Fig.4

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The pr sent inv ntion relates to clock generators for magnetic disk drives, and more particularly, to a clock generator suitabl for use, for example, in a zone-bit-recording type magnetic disk drive to assist in preventing failure (false) lock (i.e. hangup in phase-lock loops).

In the field of magnetic disk drives, recent years have seen increases in the recording density aimed at a reduction in the device size and an increase in the recording capacity, resulting in more intersymbol interference of a read signal. To deal with this, over the past few years, magnetic disks of a partial-response type utilizing intersymbol interference have been brought into practical use. In a partial-response type magnetic disk drive, if a determination point (i.e., sampling point) differs from a signal point of a read signal waveform (i.e., time at which an eye of an eye-pattern opens widest), the error rate increasingly deteriorates. Hence, in order to suppress a timing difference between the signal point and the determination point as much as possible, a clock is reproduced directly from a sampling read signal. The reliability of a clock generator of the magnetic disk drive in recovering the clock timing therefore needs to be improved.

Figure 1 shows a structure of a clock generator 60 of a previously-considered magnetic disk drive. A read signal read by a head H from a magnetic disk D in which data are recorded is amplified by an amplifier AP and partially equalized by a partial-response equalizing circuit PE to become an equalized read signal EQ which will be given to a sample-holder circuit 61.

The sample-holder circuit 61 generates a sampling signal Yn from the partially equalized read signal EQ. The sampling signal Yn is given to a partial-response phase-comparison circuit 90 and a data detection part 70. The partial-response phase-comparison circuit 90 comprises a ternary detection circuit 62, a sample-holder circuit 63, a flip-flop 64, multipliers 65 and 66, and a subtracter 67. The sampling signal Yn is supplied to the sample-holder circuit 63 which serves as means for delaying the sampling signal Yn and also to the ternary detection circuit 62.

The ternary detection circuit 62 detects three magnitude values in the sampling signal Yn, i.e., +1, 0 and -1, and generates a detection signal Xn which will be given to the first multiplier 65 and to the flip-flop 64 which serves as means for delaying the detection signal Xn. The sample-holder circuit 63 holds the sampling signal Yn received therein until receipt of a sampling clock so as to generate a delayed sampling signal Yn-1 which is delayed in time by 1 symbol. The flip-flop 64 holds the detection signal Xn received therein until receipt of the same sampling clock signal to thereby generate a delayed detection signal Xn-1 which is delayed in time by 1 symbol.

The delayed sampling signal Yn-1 and the detection signal Xn ar fed to the first multiplier 65 where they are multiplied whil the sampling signal Yn and the delayed det ction signal Xn-1 are given to the second multiplier 66 where they are multipli d. Products calculated at th first and the second multipliers 65 and 66 are given to the subtracter 67 which then calculates the difference between the products given thereto, then the difference is multiplied to thereby detect a phase difference Zn between the sampling clock pulse and the real signal point of the read signal waveform. The phase difference Zn is expressed by the equation below which is described in the literature titled "Timing recovery in digital synchronous receivers" (IEEE TRANSACTION COMMUNICATIONS, VOL. COM-24, No. 5, May 19, p.516-p.531):

$$Zn = -(Yn-1 * Xn) + (Yn * Xn-1) \quad (1)$$

The phase difference Zn is smoothed by a loop filter 68. The phase difference Zn thus smoothed controls the frequency of a voltage-controlled oscillator 69 and the voltage-oontrolled oscillator 69 outputs a clock signal. The sampling clock timing obtained in this manner is fed back to the sample-holder circuits 61 and 63, the flip-flop 64 and the data detection part 70. Sampling by the sample-holder circuits 61 and 63 and resetting of data by the flip-flop 64 are performed under the control of the same clokc timing. At the same time, this clock is given to the data detection part 70 which reproduces data from the sampling signal Yn (e.g., a data detection part for detection data by maximum likelihood detection) and used for reproduction of data.

To increase the speed of recovering this clock timing, in an preamble portion of the data, the following repetition sequences

+1, +1, -1, -1, +1, +1, -1, -1 ...

is written as a training signal and the clock is reproduced at acquisition for clock recovery from the preamble portion as is customarily done. Besides, the data are recorded on the disk D by a so-called zone-bit recording method to enhance the recording density of the data on the disk.

Figure 2A is a view showing distribution of recording units U in a recording track Tin of an inner periphery of the disk D and a recording track Tout of an outer periphery of the disk D within a previously-considered zone-bit recording type magnetic disk drive. In the zone-bit recording method, as shown in Fig. 2A, the density of magnetic recording is entirely constant from the inner recording track Tin to the outer recording track Tout and therefore the outer recording track Tout includes the greatest number of the recording units U. Figure 2B shows the format of recorded data in each recording unit U of Fig. 2A. Each recording unit U includes a preamble portion in which the training signal is written and a data portion in which the data are recorded.

Figur 3A is a waveform diagram showing the waveform of the training signal written in the preamble portions of Fig. 2B as it is read at the out r track

Tout while Fig. 3B is a waveform diagram showing the waveform of the training signal writt n in the pr amble portions of Fig. 2B as it is read at the inner track Tin. For example, in case where the number of the r - cording units U of the outer track Tout is double that of the inner track Tin in Fig. 2A, the frequency of the waveform of the training signal read at the outer track Tout is double that of the training signal read at the inner track Tin.

Assume in Figs. 3A and 3B that the points indicated at ● are normal signal points at which the clock signal is hungup and the points indicated at □ are signal points at which the clock generator is hungup as shown in Fig. 3C, at the outer track Tout, the normal frequency is 4f and the hangup frequency is 2f while at the inner track Tin, the normal frequency is 2f and the hangup frequency is f.

However, in a clock generator previously-considered for use in a zone-bit recording type magnetic disk drive, as shown in Fig. 3C, the hangup frequency 2f at the outer track Tout is equal to the hangup frequency 2f at the inner track Tin. Hence, during acquisition for clock recovery using the read signal in preamble portions of the outer track Tout, hangup occurs at the point at which the frequency is 2f, in which case normal clock recovery becomes impossible.

The reason why this hangup occurs is because in Equation 1 above for detection of the phase difference Zn, even though the sampled read signals Yn and Yn-1 are both at the level ± 1, the phase difference Zn appears to be eliminated.

In an effort to solve this problem, the present inventor has paid attention to a fact that in a zone-bit-recording type magnetic disk drive, the read signal waveform of the training signal which is recorded in the preamble portion of the data is a sinusoidal waveform. The present inventor has found that the clock signal can be extracted as a continuous signal having an analog waveform without performing sampling from the read signal waveform of the training signal.

It is desirable to provide a clock generator of a magnetic disk drive in which the problem in the above-described clock generator in a magnetic disk drive is absent.

According to an embodiment of a first aspect of the present invention, there is provided a clock generator for a magnetic disk drive in which data is recorded by the zone-bit recording method, a read signal read from a magnetic disk in which a training signal is recorded in a preamble portion of the data is sampled after partial equalizing to thereby generate a sampling read signal from which data and a clock are reproduced, the clock generator comprising: a sampl -holder circuit for gen rating a sampling signal from a r ad signal; a partial-respons phase-comparator comprising: a ternary detection circuit for detecting thre magnitude values +1, 0 and - 1 of th sampling signal to thereby generat a det ction signal; first delay means for generating a delayed sampling signal which is delayed in time by 1 symbol from the sampling signal; second delay means for generating a delayed sampling signal which is delayed in time by 1 symbol from the detection signal Xn; a first multiplier for multiplying the delayed sampling signal and the detection signal; a second multiplier for multiplying the sampling signal and the delayed sampling signal; and a subtracter for calculating the difference between the products which are obtained in the first and the second multipliers and for detecting a phase difference between a clock and a signal point of a read signal waveform; a loop filter for smoothing the phase difference signal which is detected; a voltage-controlled oscillator the frequency of which is controlled by the phase difference which is smoothed; a frequency divider for frequency dividing a signal output of the voltage-controlled oscillator; a clock extraction circuit for extracting a clock component from the training signal as it is partially equalized; a phase-comparator for comparing the phase of an output signal of the frequency divider with the phase of an output signal of the clock extraction circuit to thereby obtain a phase difference; and a change-over switch which is disposed between the partial-response phase-comparator, the phase-comparator and the loop filter, the change-over switch connecting the phase-comparator to the loop filter during reproduction of the preamble portion of the data and for connecting the partial-response phase-comparator to the loop filter during reproduction of a data portion of the data.

In such a clock-generator for a magnetic disk drive, the clock component is extracted from the training signal which is reproduced from the preamble portion of the data of the disk and which becomes a sinusoidal waveform which is 1/4 of the frequency of the clock frequency after partial equalization, and the phase of this clock component is compared with the phase of the clock which is obtained by frequency dividing the output signal of the voltage-controlled oscillator to thereby find the phase difference between the two. During reproduction of the preamble portion of the data, the phase difference thus obtained is smoothed by the loop filter and used to control the frequency of the voltage-controlled oscillator and synchronizing with a normal clock frequency is therefore performed. This frequency is different from the hangup frequency. Hence, even when a clock synchronous system is switched to the partial-response phase-comparator after detection of the preamble portion of the data, normal recovery can be continuously performed. As a result,a possibility that a clock will be generated by a hangup signal is eliminated.

In a clock generator for a magnetic disk driv embodying th present invention, hangup would not occur and therefore accurate clock reproduction is performed since after synchronizing a PLL (phase lock

loop) system which is compris d of a loop filter and a voltage-controlled oscillator with a hangup frequency using a clock component which is xtracted from a training signal which is read from a preamble portion of data, the loop is switched to hangup by means of a sampled read signal Yn.

Reference will now be made, by way of example, to the accompanying drawings, wherein:

Fig. 1 is a block circuit diagram showing an example of the structure of a previously-considered clock generator for use in a magnetic disk drive;

Fig. 2A is an explanatory diagram showing the distribution of the recording units in the recording tracks of the inner and the outer peripheries of the disk of a magnetic disk drive of the zone-bit recording type;

Fig. 2B is an explanatory diagram showing the format of recorded data in each recording unit;

Fig. 3A is a waveform diagram showing the waveform of the training signal written in the preambles as those shown in Fig. 2B as it is read at the outer periphery;

Fig. 3B is a waveform diagram showing the waveform of the training signal written in the preambles as those shown in Fig. 2B as it is read at the inner periphery;

Fig. 3C is a view explaining the relationship between the hangup frequencies by means of the training signal and the hangup frequency;

Fig. 4 is a view showing parts of a clock generator for a magnetic disk drive embodying the present invention;

Fig. 5 is a block circuit diagram showing parts of a clock generator according to a first embodiment of the present invention;

Figs. 6A and 6B are waveform diagrams showing operating waveforms of parts shown in Fig. 5;

Fig. 5;

Figs. 7A to 7C are waveform diagrams showing operating waveforms of parts shown in Fig. 5;

5;

Fig. 8 is a block circuit diagram showing parts of a clock generator according to a second embodiment of the present invention;

Figs. 9A to 9C are waveform diagrams showing operating waveforms of parts shown in Fig. 8;

Fig. 10 is a block circuit diagram showing parts of a clock generator according to a third embodiment of the present invention;

Figs. 11A to 11E are waveform diagrams showing operatins waveforms of parts shown in Fig. 10;

Fig. 12 is a block circuit diagram showing parts of a clock generator according to a fourth embodiment of th present invention; and

Figs. 13A and 13B are waveform diagrams showing operating wav forms of parts shown in Fig. 12.

Figure 4 is a block diagram showing parts of a clock generator for a magnetic disk drive embodying the present invention.

In Fig. 4, the elements that have th same functions as elements in Fig. 1 are assigned the same reference numerals.

In a magnetic disk drive in which the Figure 4 clock generator is used, data are recorded by the zone-bit recording method; a read signal read from a magnetic disk in which a training signal is recorded in a preamble portion of the data is sampled after partial equalizing; and data and a clock are reproduced from the sampled read signal.

The Figure 4 clock generator has the following elements which correspond to those in the previously-considered clock generator of Figure 1: a sample-holder circuit 61; a partial-response phase-comparator 90 having a ternary detection circuit 62, a sample-holder circuit 63, a flip-flop 64, multipliers 65 and 66, and a subtractor 67; a loop filter 68; a voltage-controlled oscillator 69; a data detection part 70.

A frequency divider 11, a clock extraction circuit 12, a phase-comparator 13 and a change-over switch 14, none of which are included in the Figure 1 clock generator, are provided in the Figure 4 clock generator.

The sample-holder circuit 61 generates a sampling signal Yn from the read signal. The ternary detection circuit 62 detects three magnitude values +1, 0 and -1 of the sampling signal Yn and generates a detection signal Xn. The sample-holder circuit 63 generates a delayed sampling signal Yn-1 which is delayed in time by 1 symbol from the sampling signal Yn. The flip-flop 64 generats a delayed sampling signal Xn-1 which is delayed in time by 1 symbol from the detection signal Xn. The multiplier 65 multiplies the delayed sampling signal Yn-1 and the detection signal Xn, and the multiplier 66 multiplies the sampling signal Yn and the delayed sampling signal Xn-1. The subtracter 67 calculats the difference between the products obtained from the multipliers 65 and 66 and detects a phase difference Zn between a clock and signal point of a read signal waveform. The loop filter 68 smoothes the detected phase difference Zn. The frequency of the voltage-controlled oscillator 69 is controlled by the smoothed phase difference Zn.

The frequency divider 11 divides the signal from the voltage-controlled oscillator 69 and supplies the same to the phase-comparator 13. The phase-comparator 13 compares the phase of an output signal of the frequency divider 11 with the phase of an output signal of the clock extraction circuit 12 to obtain a phase difference. The change-over switch 14 is disposed between the partial-response phase-comparator 90, the phase-comparator 13 and the loop filter 68, and connects the phase-comparator 13 to th loop filt r 68 during reproduction of th preamble portion of the data and connects th partial-r - spons phase-comparator 90 to the loop filter 68 dur-

ing reproduction of a data portion of the data.

The function of th Figur 4 clock gen rator will be explained hereinaft rwithr fer nc to a pref rr d embodiment of the clock xtraction circuit 12.

Figure 5 is a block circuit diagram showing the structure of a clock generator 20 of a zone-bit recording type magnetic disk drive according to a first embodiment of the present invention, and shows the structure beyond the partial-response equalizing circuit PE of the clock generator 60 of the conventional magnetic disk drive described with reference to Fig. 1. The data detection part 70 is omitted. Parts similar to those previously described with reference to Fig. 1 are denoted by the same reference numerals, and similar descriptions will simply be omitted.

In the first embodiment as well, the equalized read signal EQ generated by partial equalization at the partial equalizing circuit PE is supplied to the sample-holder circuit 61 where the sampling signal Yn is generated. The read signal EQ, or the training signal partially equalized by the partial equalizing circuit PE, has a sinusoidal waveform which is 1/4 of the frequency of the clock CLK as shown in Figs. 6A, 6B, 7A, 7B, and 7C. On the other hand, the sampling signal Yn generated by the sample-holder circuit 61 has a rectangular waveform.

The sampling signal Yn is given to a partial-response phase-comparator 90 which comprises the sample 63, the flip-flop 64, the multipliers 65 and 66,and the subtracter 67 as shown in Fig. 6. Likewise in the conventional magnetic disk drive, in the partial-response phase-comparator 90, three magnitude values of the sampling signal Yn, i.e., +1, 0 and -1 are detected so that the detection signal Xn is created, the delayed sampling signal Yn-1 which is delayed in time by 1 symbol is generated from the sampling signal Yn by the sample-holder circuit 63, and the delayed detection signal Xn-1 which is delayed in time by 1 symbol is generated from the detection signal Xn by the flip-flop 64. Following this, the delayed sampling signal Yn-1 and the detection signal Xn are multiplied while the sampling signal Yn and the delayed detection signal Xn-1 are multiplied respectively in the multipliers 65 and 66. The products thus calculated are supplied to the subtracter 67 so that phase difference Zn between the clock and the signal point of the read signal waveform is detected as in the Figure 1 magnetic disk drive.

On the other hand, the equalized read signal EQ generated by partial equalization at the partial equalizing circuit PE (not shown) is also supplied to a zero crossing detection circuit 21 which is disposed parallel to the sample-holder circuit 61 as a clock extraction circuit. Th z ro crossing detection circuit 21 extracts timings at which the training signal crosses the level 0 and generates a rectangular wav form indicated at B which will b th n s nt to a phas -comparator 22, as shown in Fig. 6B.

As described earlier, since the qualized read signal EQ obtained from the training signal is a sinusoidal waveform which is 1/4 of th fr quency of the clock CLK, in this mbodiment, th clock output CLK from the voltage-controlled oscillator 69 which will be described later is frequency divided by four by a quarter frequency divider 23 and sent to the phase-comparator 22. The phase-comparator 22 compares the phase of the clock which is generated by extracting the timing at which the training signal crosses the level 0 with the phase of the clock which is created by frequency dividing the output signal of the voltage-controlled oscillator 69 by four, and outputs a phase difference Tn.

The phase difference Zn from the partial-response phase-comparator 90 and the phase difference Tn from the phase-comparator 22 are respectively given to two input terminals of a change-over switch 80 in such a manner that either one output will be received by the loop filter 68. In this embodiment, the change-over switch 80 connects the loop filter 68 to the phase-comparator 22 during reproduction of the preamble portion of data and connects the loop filter 68 to the partial-response phase-comparator 90 during reproduction of the data portion of the data.

Hence, during reproduction of the preamble portion of data, the phase difference Tn between the clock which is generated by extracting the timings at which the training signal crosses the level 0 and the clock which is created by frequency dividing the output signal of the voltage-controlled oscillator 69 by four is sent from the phase-comparator 22 to the loop filter 68 through the change-over switch 80 so that the frequency of the voltage-controlled oscillator 69 is synchronized with the normal frequency. At this stage, the frequency of the voltage-controlled oscillator 69 is clearly different from the hangup frequency by the sampling signal. Hence, even when the change-over switch 80 has changed its connection to the partial-response phase-comparator 90 and the clock generation system has changed to hangup by means of the sampling signal during reproduction of the data portion that follows, normal hangup continues.

Figure 8 is a block circuitry diagram showing a structure of a clock generator 30 of a zone-bit-recording-type magnetic disk drive according to a second embodiment of the present invention. The clock generator 30 differs from the clock generator 20 of the magnetic disk drive according to the first embodiment described with reference to Fig. 5 in relation to the structure of a clock extraction circuit 12. Parts similar to those previously described with reference to Fig. 5 ar d not d by the same reference numerals, and similar description will be simply be omitted.

In th second embodiment, the clock xtraction circuit 12 is comprised of an absolut value circuit 31, an envelope d tect circuit 32 and a comparator 33.An

output of the comparator 33 is given to the phase-comparator 22 which receiv s at its other input an output of a fr qu ncy divider 23'.

In the second embodiment as well, the qualized read signal EQ which is generated by partially equalizing the training signal in the partial equalizing circuit PE (not shown) has sinusoidal waveform which is 1/4 of the frequency of the clock CLK as shown in Figs. 6A, 6B, 7A, 7B, and 7C. On the other hand, the sampling signal Yn, which is created by the sample-holder circuit 61, has a rectangular waveform.

The partially equalized read signal EQ is also given to the absolute value circuit 31 and the envelope detection circuit 32 which are disposed parallel to the sample-holder circuit 61. At the absolute value circuit 31, as shown in Fig. 8, negative portions of the training signal are inverted so that a rectifying wave as indicated at C is created which will be supplied to the comparator 33. Since the equalized read signal EQ, i.e., the training signal as it is partially equalized, is a sinusoidal waveform, the envelope detection circuit 32 detects the levels ± 1 as an envelope which will be then fed to the comparator 33.

The comparator 33 compares the signal received from the absolute value circuit 31 with the levels ± 1 so that a rectangular wave similar to that indicated at D in Fig. 9C is developed and inputted to the phase-comparator 22. As described earlier, although the equalized read signal EQ of the training signal is a sinusoidal waveform which is 1/4 of the frequency of the clock CLK, since the equalized read signal EQ of the training signal is rectified by the absolute value circuit 31, the clock signal extracted from the equalized read signal EQ of the training signal after rectification is 1/2of the frequency of the clock CLK. Hence, in this embodiment, the clock output CLK of the voltage-controlled oscillator 69 which will be described later is frequency divided by 2 by a half frequency divider 23' and given to the phase-comparator 22.

The phase-comparator 22 compares the phase of the rectangular which is received from the comparator 33 with the phase of the clock which is created by frequency dividing the output signal of the voltage-controlled oscillator 69 by 2, and outputs a phase difference Un.

The phase difference Zn from the partial-response phase-comparator 90 and the phase difference Un from the phase-comparator 22 are respectively sent to two input terminals of the change-over switch 80 in such a manner that either one output will be received by the loop filter 68. In this embodiment,the change-over switch 80 connects the loop filter 68 to the phase-comparator 22 during reproduction of th pr amble portion of data and connects the loop filt r 68 to the partial-respons phase-comparator 90 during r production of the data portion of th data.

Hence, during reproduction of the preambl portion of data, the phas difference Un between the clock which is generated by comparing the envelop of the training signal and the absolute value and the clock which is created by frequency dividing the output signal of the voltage-controlled oscillator 69 by 2 is sent from the phase-comparator 22 to the loop filter 68 through the change-over switch 80 so that the frequency of the voltage-controlled oscillator 69 is synchronized with the normal frequency which is different from the hangup frequency by the sampling signal. Hence, even when the change-over switch 80 has changed its connection to the partial-response phase-comparator 90 and the clock generation system has changed to hangup by means of the sampling signal during reproduction of the data portion that follows, continuation of hangup is ensured.

Figure 10 is a block circuit diagram showing a structure of a clock generator 40 of a zone-bit-recording-type magnetic disk drive according to a third embodiment of the present invention. The clock generator 40 differs from the clock generator 20 in the magnetic disk drive according to the first embodiment described with reference to Fig. 5 in relation to the structure of a clock extraction circuit 12. Parts similar to those previously described with reference to Fig. 5 are denoted by the same reference numerals, and similar descriptions will simply be omitted.

In the third embodiment, the clock extraction circuit 12 is comprised of first and second comparators 41 and 42, an envelope detection circuit 43 and an exclusive OR circuit 44. An output of the exclusive OR circuit 44 is sent to the phase-comparator 22 which receives at its other input an output of the frequency divider 23'.

In the third embodiment, the equalized read signal EQ which is generated by partially equalizing the training signal at the partial-response equalizing circuit PE (not shown) has a sinusoidal waveform which is 1/4 of the frequency of the clock CLK as shown in Figs. 6A, 6B, 7A, 7B, and 7C. On the other hand, the sampling signal Yn which is created by the sample-holder circuit 61 has a rectangular waveform.

The partially equalized read signal EQ is also given to one inputs of the first and the second comparators 41 and 42 and the envelope detection circuit 43 which are disposed parallel to the sample-holder circuit 61. Since the equalized read signal EQ, i.e., the training signal as it is partially equalized, is a sinusoidal waveform, the envelope detection circuit 43 detects the levels ± 1 as an envelope. The +1 level is supplied to other input of the first comparator 41 and the -1 level is supplied to other input of the second comparator.

Th first comparator 41 compares the qualized read signal EQ with the +1 level and generates a rectangular wav similar to that indicated at E in Fig. 11A which will be then supplied to th exclusive OR circuit 44. The second comparator 42 compar s the qual-

ized read signal EQ with the -1 level and generates a rectangular wav similar to that indicated at F in Fig. 11B which will be then supplied to the exclusiv OR circuit 44. The exclusive OR circuit 44 calculates an exclusive OR of the two signals received therein and generates a rectangular wave, similar to that indicated at G in Fig. 11D which will be supplied to the phase-comparator 22.

Although the equalized read signal EQ of the training signal is a sinusoidal waveform which is 1/4 of the frequency of the clock CLK and the outputs of the first and the second comparators 41 and 42 are 1/4 of the frequency of the clock CLK, since the exclusive OR of the outputs of the first and the second comparators 41 and 42 is calculated by the exclusive OR circuit 44, the clock signal extracted from the equalized read signal EQ of the training signal after calculation of the exclusive OR is 1/2 of the frequency of the clock CLK. Hence, in this embodiment, the clock output CLK of the voltage-controlled oscillator 69 which will be described later is frequency divided by 2 by the half frequency divider 23' and given to the phase-comparator 22.

The phase-comparator 22 compares the phase of the rectangular wave which is received from the exclusive OR circuit 44 with the phase of the clock which is created by frequency dividing the output signal of the voltage-controlled oscillator 69 by 2, and outputs the phase difference Un which will be given to two input terminals of the change-over switch 80. In this embodiment, too, the change-over switch 80 connects the loop filter 68 to the phase-comparator 22 during reproduction of the preamble portion of data and connects the loop filter 68 to the partial-response phase-comparator 90 during reproduction of the data portion of the data.

Hence, during reproduction of the preamble portion of data, the phase difference Un between the clock which is generated from the training signal as it is and as it is compared with the envelope and which is synthesized at the exclusive OR circuit 44 and the clock which is created by frequency dividing the output signal of the voltage-controlled oscillator 69 by 2 is sent from the phase-comparator 22 to the loop filter 68 through the change-over switch 80 so that the frequency of the voltage-controlled oscillator 69 is synchronized with the normal frequency which is different from the hangup frequency by the sampling signal. Hence, even when the change-over switch 80 has changed its connection to the partial response phase-comparator 90 and the clock generation system has changed to hangup by means of the sampling signal during reproduction of the data portion that follows, continu d normal hangup is assur d.

Figure 12 is a block circuit diagram showing a structur of a clock generator 50 of a zon -bit recording type magnetic disk driv according to a fourth mbodiment of th pr sent invention. The clock generator 50 differs from the clock generator 20 of the magnetic disk drive according to th first embodiment described with r ferenc to Fig. 5 in that the zero crossing detection circuit 21 is replaced with a peak detection circuit 51. Parts similar to those previously described with reference to Fig. 5 are denoted by the same reference numerals,and similar description will be simply be omitted.

In the fourth embodiment, the partially equalized read signal EQ is also sent to the peak detection circuit 51 which is disposed in parallel to the sample-holder circuit 61. As indicated at H in Figs. 12 and 13A, the peak detection circuit 51 generates a rectangular wave which rises at positive and negative peaks of the training signal and the rectangular wave is inputted to the phase-comparator 22. The phase-comparator 22 receives at its other input an output of the frequency divider 23'.

In the fourth embodiment as well, the equalized read signal EQ which is generated by partially equalizing the training signal at the partial-response equalizing circuit PE (not shown) has a sinusoidal waveform which is 1/4 of the frequency of the clock CLK as shown in Figs. 6A, 6B, 7A, 7B, and 7C. On the other hand, the sampling signal Yn which is created by the sample-holder circuit 61 has a rectangular waveform. The equalized read signal EQ of the training signal is a sinusoidal waveform which is 1/4 of the frequency of the clock CLK, while the rectangular wave which rises at the positive and the negative peaks of the training signal is 1/2 of the frequency of the clock CLK. Hence, in this embodiment, the clock output CLK of the voltage-controlled oscillator 69 which will be described later is frequency divided by 2 by the half frequency divider 23' and sent to the phase-comparator 22. The phase-comparator 22 compares the phase of the rectangular wave which is received from the peak detection circuit 51 with the phase of the clock which is created by frequency dividing the output signal of the voltage-controlled oscillator 69 by 2, and outputs the phase difference Un.

The phase difference Zn from the partial-response phase-comparator 90 and the phase difference Un from the phase-comparator 22 are respectively given to two input terminals of the change-over switch 80 in such a manner that either one output will be received by the loop filter 68. In this embodiment, the change-over switch 80 connects the loop filter 68 to the phase-comparator 22 during reproduction of the preamble portion of data and connects the loop filter 68 to the partial-response phase-comparator 90 during reproduction of the data portion of the data.

Hence, during reproduction of the preamble portion of data, the phas differ nce Un b tween the clock which is generated using the p ak values of the training signal and the clock which is creat d by frequency dividing the output signal of the voltage-controlled oscillator 69 by 2 is sent from th phase-

comparator 22 to th loop filter 68 through the change-over switch 80 so that the frequency of the voltage-controlled oscillator 69 is synchronized with th normal frequency which is different from the hangup frequency by the sampling signal. Hence, even when the change-over switch 80 has changed its connection to the partial-response phase-comparator 90 and the clock synchronous system has changed to clock recovery by means of the sampling signal during reproduction of the data portion that follows, continued normal recovery is assured.

As heretofore described, in a clock generator embodying the present invention, during reproduction of the preamble portion of data the frequency of the voltage-controlled oscillator 69 is controlled by the clock which is generated from the read signal which is not sampled during reproduction of the data portion, clock generation is performed using the sampling signal Yn. Hence, there is no possibility that the clock will be hungup.

As described above, in a clock generator embodying the present invention, since the clocks generated in a different clock synchronous system during reproduction of the preamble portion of data, hangup would not occur, and therefore, accurate clock reproduction is performed. In addition, since synchronizing with the sampling signal is carried out after hanging up the frequency by means of the continuous signal obtained from the training signal which is written in the preamble portion of the data, the clock is recovered quickly.

Claims

1. A clock generator for a magnetic disk drive, in which data are recorded by the zone-bit recording method, in which a read signal is read from a magnetic disk in which a training signal is recorded in a preamble portion of the data and is sampled, after partial equalizing, to thereby generate a sampling read signal from which data and a clock are reproduced, said clock generator comprising:

   a sample-holder circuit (1) for generating a sampling signal (Yn) from a read signal; a partial-response phase-comparator (10) comprising: a ternary detection circuit (2) for detecting three magnitude values +1, 0 and -1 of said sampling signal (Yn) to thereby generate a detection signal (Xn); first delay means (3) for generating a delayed sampling signal (Yn-1) which is delayed in time by 1 symbol from said sampling signal (Yn); second delay means (4) for gen rating a delayed det ction signal (Xn-1) which is delay d in time by 1 symbol from said detection signal (Xn); a first multiplier (5) for multiplying said delayed sampling signal (Yn-1) and said detection signal (Xn); a second multipli r (6) for multiplying said sampling signal (Yn) and said delay d detection signal (Xn-1); and a subtracter (7) for calculating the difference b tween th products which are obtained in said first and said second multipliers (5) and (6) and for detecting a phase difference (Zn) between a sampling clock timing and a signal point of a read signal waveform; a loop filter (8) for smoothing the phase difference (Zn) which is detected; and a voltage-controlled oscillator (9) the frequency of which is controlled by the phase difference (Zn) which is smoothed;

   characterised in that said clock generator further comprises:

   a frequency divider (11) for frequency dividing a signal from the voltage-controlled oscillator (9);

   a clock extraction circuit (12) for extracting a clock component from said training signal as it is partially equalized;

   a phase-comparator (13) for comparing the phase of an output signal of the frequency divider (11) with the phase of an output signal of the clock extraction circuit (12) to thereby obtain a phase difference; and

   a change-over switch (14) which is disposed between said partial-response phase-comparator (10), said phase-comparator (13) and said loop filter(8), said change-over switch (14) connecting said phase-comparator (13) to said loop filter (8) during reproduction of the preamble portion of the data and for connecting said partial-response phase-comparator (10) to said loop filter (8)during reproduction of a data portion of the data.

2. A clock generator for a magnetic disk drive as set forth in claim 1, wherein said clock extraction circuit (12) is a zero-crossing detector which extracts timings at which said training signal crosses a 0 level and said frequency divider (11) is a quarter frequency divider.

3. A clock generator for a magnetic disk drive as set forth in claim 1, wherein said clock extraction circuit (12) is comprised of an absolute value circuit for detecting the absolute value of said training signal, an envelope detection circuit for detecting the amplitude of said training signal and a comparator for comparing output signals of said absolute value circuit and said envelope detection circuit, and said frequency divider (11) is a half frequency divider.

4. A clock generator for a magnetic disk drive as set forth in claim 1, wherein said clock xtraction circuit (12) is comprised of an envelope d tection circuit for detecting the amplitude of said training

signal, a first comparator for comparing a +1 level output signal of the env lop detection circuit with said training signal, a second comparator for comparing a -1 level output signal of th env lope detection circuit with said training signal and an exclusive OR circuit for calculating an exclusive OR of output signals from said first and said second comparators, and said frequency divider (11) is a half frequency divider.

5. A clock generator for a magnetic disk drive as set forth in claim 1, wherein said clock extraction circuit (12) is a peak detector for detecting peaks of said training signal and said frequency divider (11) is a half frequency divider.

6. A magnetic disk drive, in which data are recorded by the zone-bit recording method, comprising means (H,AP) for reading a read signal from a magnetic disk having, recorded thereon in a preamble portion of the data, a training signal; means (61) for sampling the said read signal, after partial equalising thereof, to generate a sampling read signal (Yn) from which data and a clock are reproduced; and a clock generator including:

a partial-response phase-comparator (90) operable to detect a phase difference (Zn) between a sampling clock timing and a signal point of a read signal waveform;

a loop filter (68) for smoothing the detected phase difference (Zn); and

a voltage-controlled oscillator (69) the frequency of which is controlled by the smoothed phase difference (Zn);

characterised in that the said clock generator further includes:

a frequency divider (11) for frequency dividing a signal from the voltage-controlled oscillator (69);

a clock extraction circuit (12) for extracting a clock component from said training signal as it is partially equalised;

a phase-comparator (13) for comparing the phase of an output signal of the frequency divider (11) with the phase of an output signal of the clock extraction circuit (12) to thereby obtain a phase difference; and

a change-over switch (14) which is disposed between said partial-response phase-comparator (90), said phase-comparator (13), and said loop filter (68), said change-over switch (14) serving to connect said phase-comparator (13) to said loop filter (68) during reproduction of the preamble portion of the data and serving to connect said partial-response phase-comparator (90) to said loop filter (68) during r production of a data portion of the data.

Fig.1

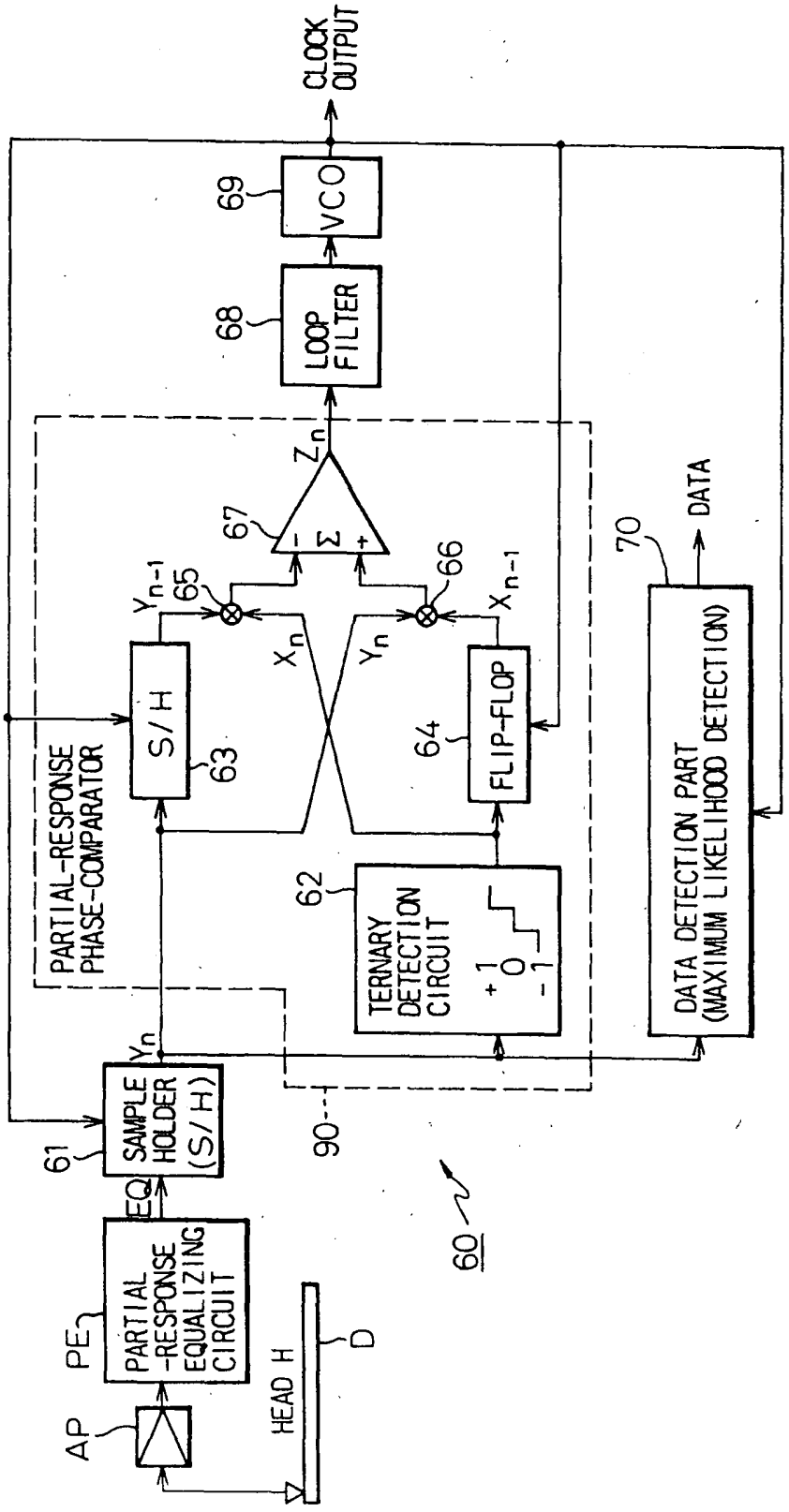
CLOCK OUTPUT
69
VCO
68
LOOP FILTER
Z_n
67
Σ
Y_{n-1}
65
66
X_{n-1}
X_n
Y_n
S/H
63
64
FLIP-FLOP
PARTIAL-RESPONSE PHASE-COMPARATOR
62
TERNARY DETECTION CIRCUIT
+1
0
-1
70
DATA
DATA DETECTION PART (MAXIMUM LIKELIHOOD DETECTION)
Y_n
61
SAMPLE HOLDER (S/H)
EQ
90
60
PE
PARTIAL -RESPONSE EQUALIZING CIRCUIT
AP
HEAD H
D

Fig.2A

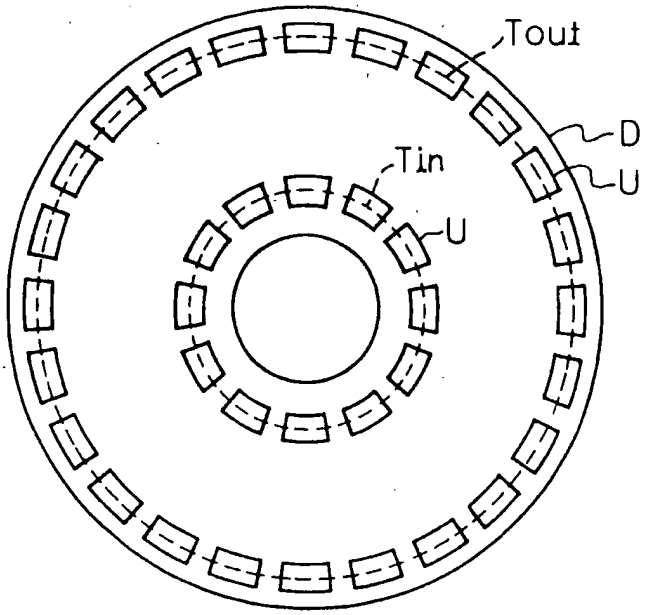
Tout
D
U
Tin
U

Fig.2B

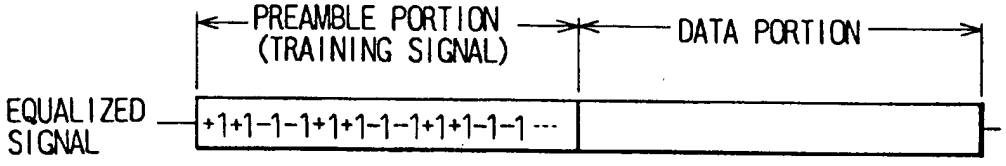
PREAMBLE PORTION
(TRAINING SIGNAL)
DATA PORTION
EQUALIZED SIGNAL
+1+1-1-1+1+1-1-1+1+1-1-1 ···

Fig.3A

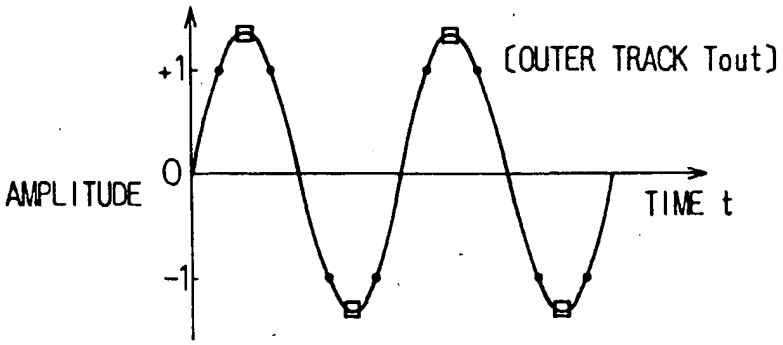

Fig.3B

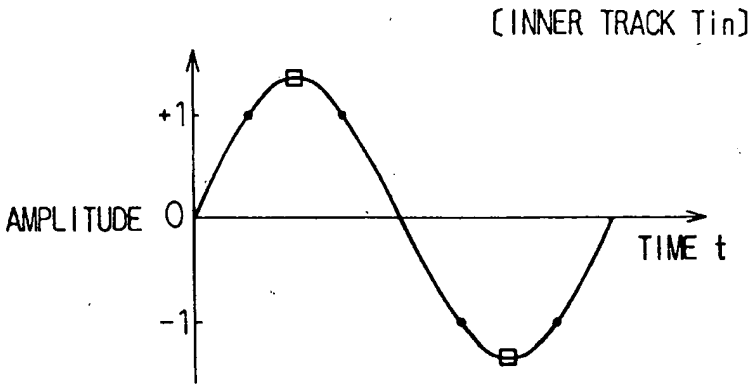

Fig.3C

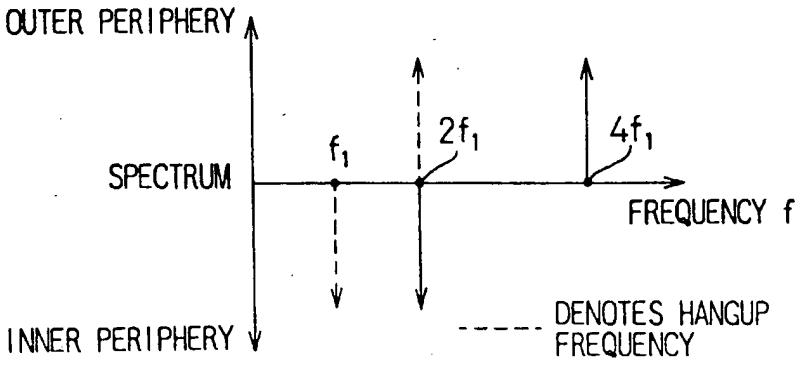

Fig.4

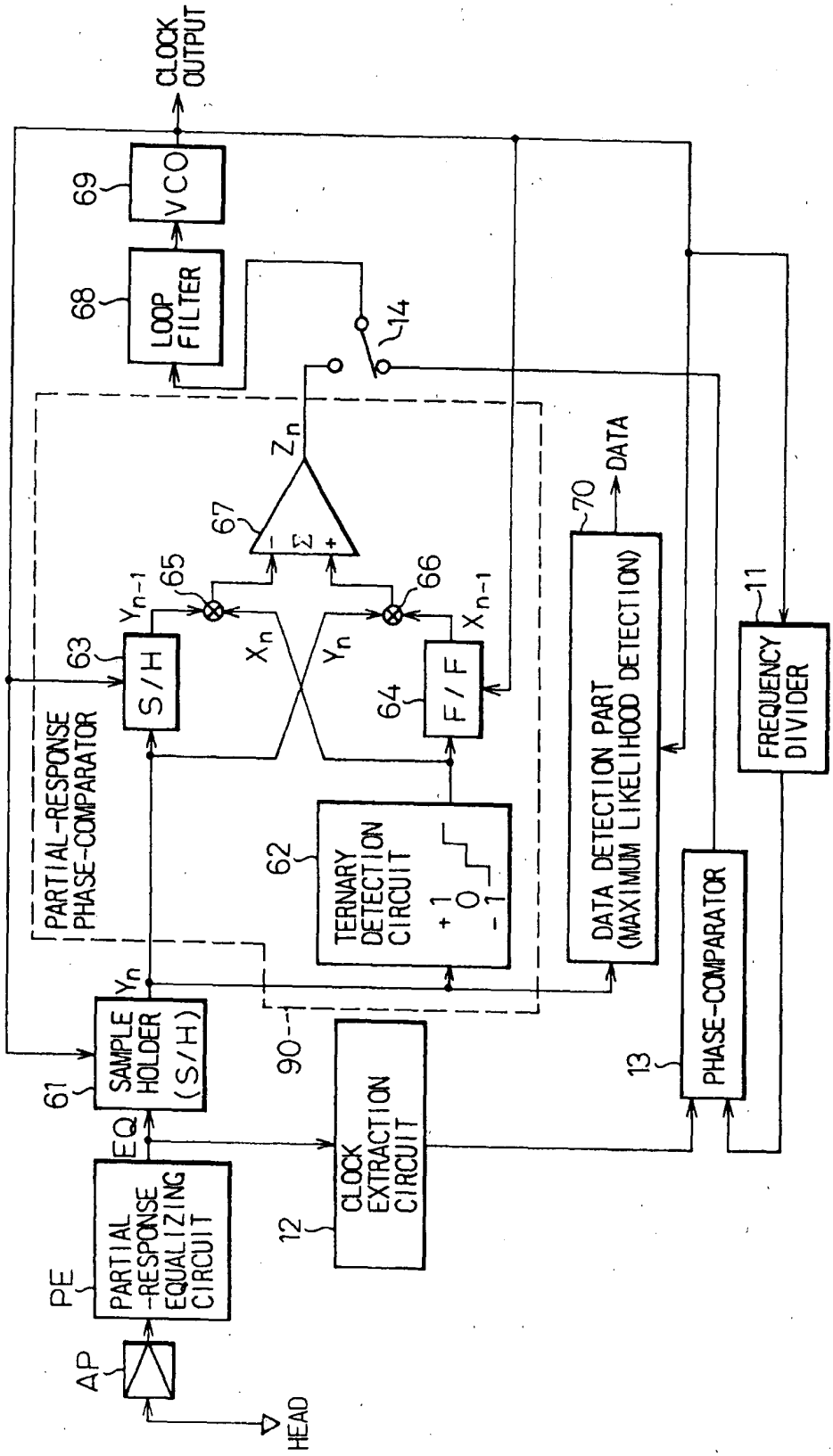
CLOCK OUTPUT
69
VCO
68
LOOP FILTER
14
Z_n
67
Σ
70
DATA
65
66
Y_{n-1}
X_{n-1}
63
S/H
X_n
Y_n
64
F/F
PARTIAL-RESPONSE PHASE-COMPARATOR
62
TERNARY DETECTION CIRCUIT
+1
0
-1
DATA DETECTION PART (MAXIMUM LIKELIHOOD DETECTION)
11
FREQUENCY DIVIDER
Y_n
61
SAMPLE HOLDER (S/H)
90
CLOCK EXTRACTION CIRCUIT
13
PHASE-COMPARATOR
EQ
PE
PARTIAL -RESPONSE EQUALIZING CIRCUIT
12
AP
HEAD

Fig.5

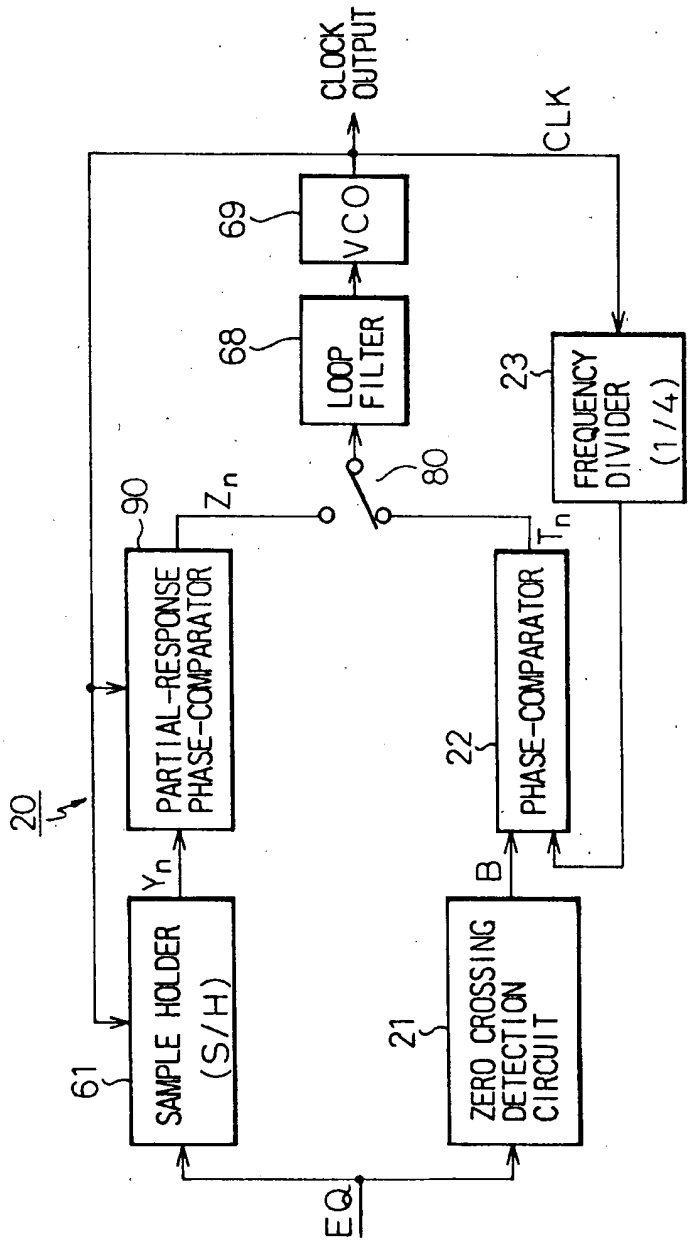
CLOCK OUTPUT
CLK
69
VCO
68
LOOP FILTER
23
FREQUENCY DIVIDER (1/4)
80
90
Z_n
T_n
PARTIAL-RESPONSE PHASE-COMPARATOR
PHASE-COMPARATOR
22
20
Y_n
B
SAMPLE HOLDER (S/H)
ZERO CROSSING DETECTION CIRCUIT
61
21
EQ

Fig.6A

Fig.6B

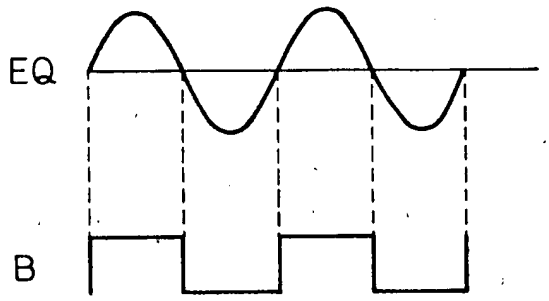

Fig.7A

Fig.7B

Fig.7C

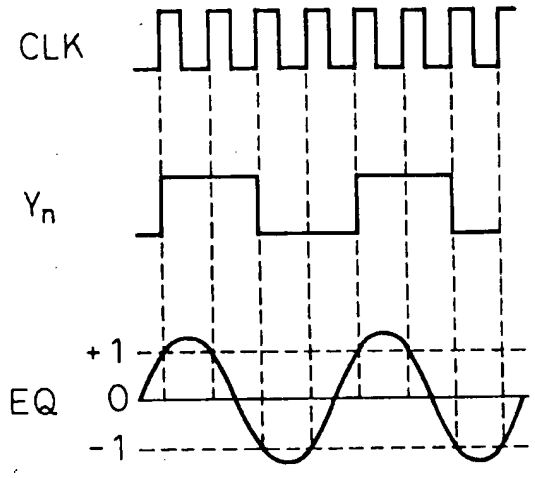

Fig.8

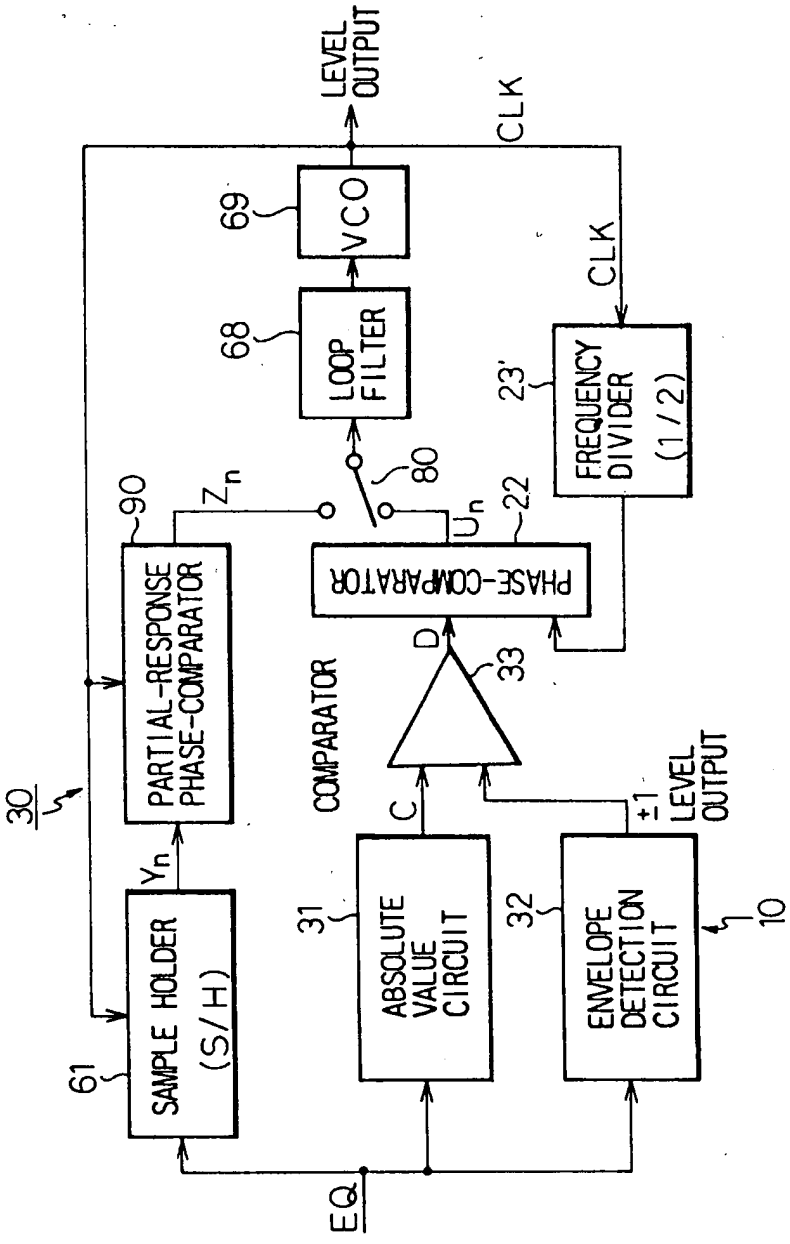
LEVEL OUTPUT
CLK
69
VCO
68
LOOP FILTER
23'
FREQUENCY DIVIDER (1/2)
CLK
90
Z_n
80
U_n
22
PHASE-COMPARATOR
PARTIAL-RESPONSE PHASE-COMPARATOR
D
33
COMPARATOR
30
C
±1 LEVEL OUTPUT
Y_n
31
ABSOLUTE VALUE CIRCUIT
32
ENVELOPE DETECTION CIRCUIT
10
61
SAMPLE HOLDER (S/H)
EQ

Fig.9A

Fig.9B

Fig.9C

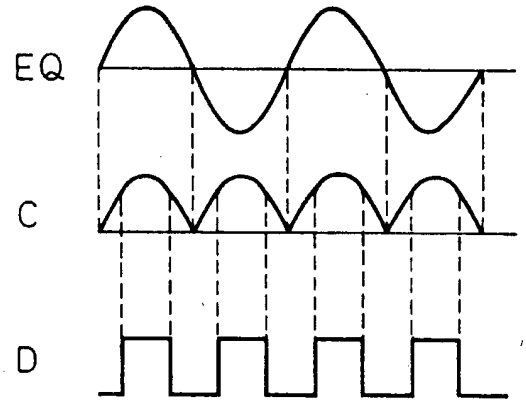

Fig.10

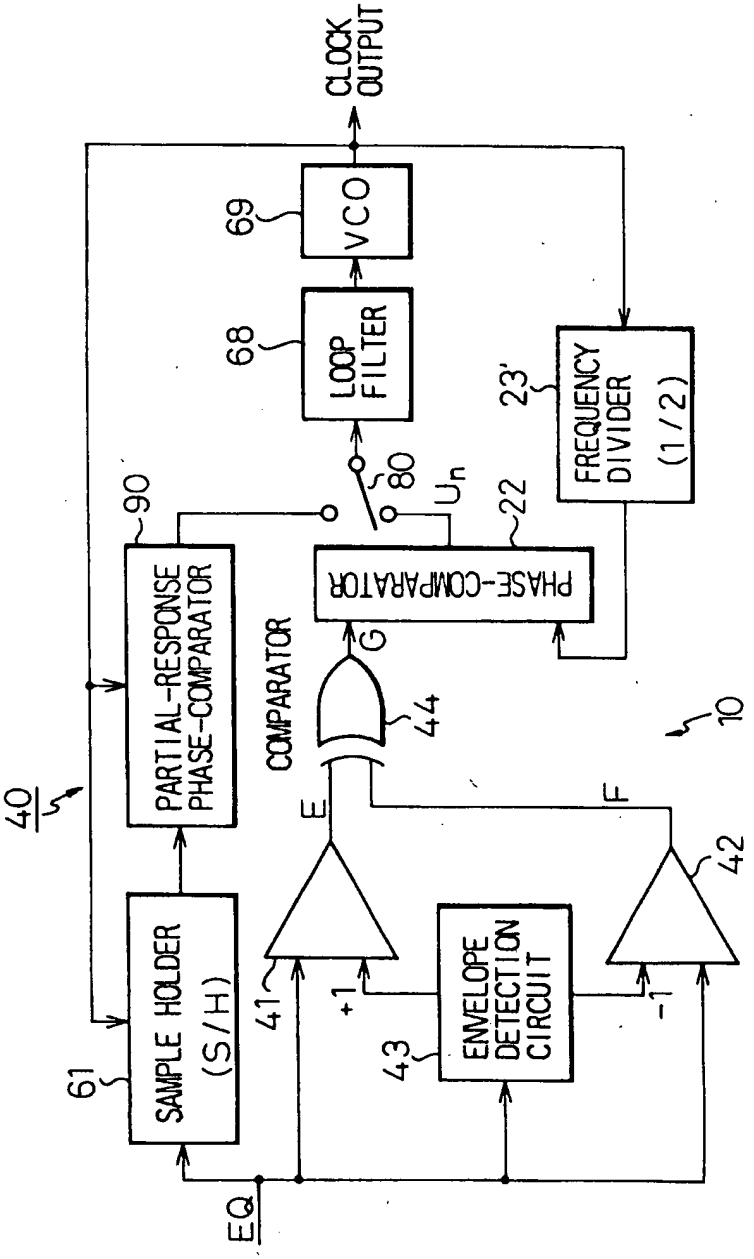
CLOCK OUTPUT
VCO
69
LOOP FILTER
68
FREQUENCY DIVIDER (1/2)
23'
80
U_n
22
90
PARTIAL-RESPONSE PHASE-COMPARATOR
PHASE-COMPARATOR
COMPARATOR
G
44
40
E
F
10
42
41
+1
-1
43
ENVELOPE DETECTION CIRCUIT
61
SAMPLE HOLDER (S/H)
EQ

Fig.11A

Fig.11B

Fig.11C

Fig.11D

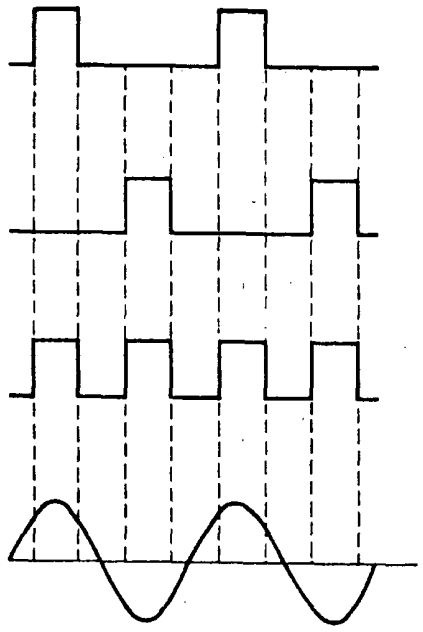

Fig.12

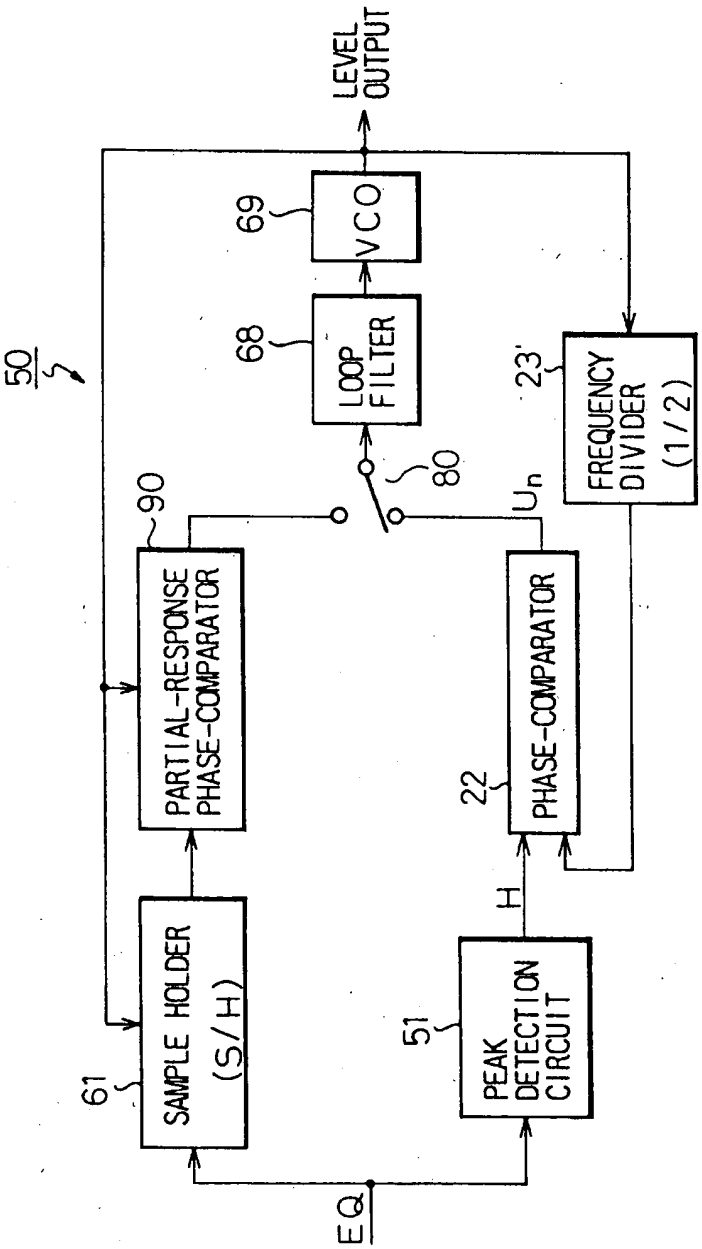
LEVEL OUTPUT
69
VCO
68
LOOP FILTER
23'
FREQUENCY DIVIDER (1/2)
50
80
90
U_n
PARTIAL-RESPONSE PHASE-COMPARATOR
22
PHASE-COMPARATOR
H
61
SAMPLE HOLDER (S/H)
51
PEAK DETECTION CIRCUIT
EQ

Fig.13A

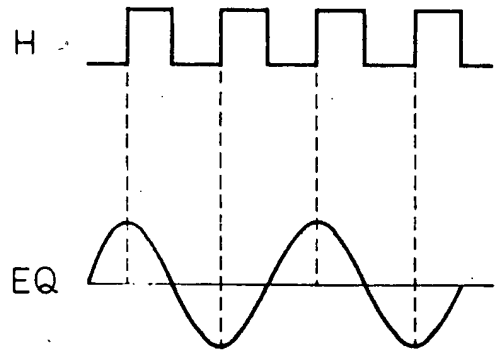

Fig.13B